IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	Pankaj K. Jha		
Application No.:	09/881,493	Examiner:	Patel, H.
Filed:	June 14, 2001	Art Group:	2154
For:	PROGRAMMABLE PROTOCOL PROCESSING ENGINE FOR NETWORK PACKET DEVICES		

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant submits the following Appeal Brief pursuant to 37 C.F.R. §41.37 for consideration by the Board of Patent Appeals and Interferences. Appellant also submits herewith a PTO-2038 Form in the amount of $500.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §41.20(b)(2). Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

This application is related to co-pending application Serial No. 09/881,367, which was received by the Technology Center at the Board of Patent Appeals and Interferences on December 8, 2006, Appeal No. 2007-0708. There are no related judicial proceedings or interferences known to the Appellant, Appellant's legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are pending and remain rejected. The Appellant hereby appeals the rejection of claims 1-20.

IV. STATUS OF AMENDMENTS

Appellant is appealing a final Office Action issued by the Examiner on August 31, 2006. On October 23, 2006, Appellant filed an Amendment After Final that amended claims 6 and 7 and requested reconsideration of all other claims. On November 28, 2006, the Examiner issued an Advisory Action indicating that the Amendment After Final changes would not be entered. On December 14, 2006, Appellant filed (i) a Notice of Appeal and (ii) a Request for Review, both based

on the claims prior to the Amendment After Final. On February 1, 2007, the Examiner issued a Notice of Panel Decision for Pre-Appeal Brief Review indicating that the case would proceed to the Board of Patent Appeals and Interferences.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A first embodiment of the present invention (as represented by claim 1) generally concerns an assembly 126 comprising a database circuit 130 and a processing circuit 128. The basic structure of the assembly 126 may be found in the specification on page 5, lines 5-16 and is illustrated in FIG. 2. The database circuit 130 may be configured to store a plurality of pointer values for a plurality of first parameters (see FIG. 5) defined by a network protocol (e.g., protocol of network 104), wherein each one of the first parameters is associated with a corresponding one of the pointer values. The pointer values are generally represented by the signal POINTER in FIG. 2 and are described in the specification on page 12, lines 14-21. The pointer values may specify how the parameters received in an incoming packet INP1 from network 104 are to be processed (specification page 13, lines 10-11). An example of the relationships of the pointer values to parameters in an Ethernet frame is shown in FIG. 5 and described in the text on page 18, lines 1-10.

The processing circuit 128 may be configured to (i) process a particular one of the first parameters in the incoming packet INP1 received by the assembly 126 in accordance with the corresponding pointer value to produce a second parameter. Processing of a particular first parameter is generally described in the specification on page 14, line 1 through page 15, line 7. Details of the internal workings of the processing circuit 128 are also shown in FIG. 3. Descriptions

of the processing performed by the peripherals 132a-132m on the parameters may be found on page 14, line 8 through page 15, line 7. The processing circuit 128 may be further configured to (ii) present an outgoing packet OUTP1 from the assembly containing the second parameter (see FIG. 5). Assembly and presentation of the outgoing packet may be performed by the assembler 136, as described in the specification on page 15, lines 8-17.

A second embodiment of the present invention (as represented by claim 10) generally concerns an assembly 100 comprising a first circuit (as represented by the network 1 interface circuit 122), a second circuit (as represented by the protocol processing engine 126) and a third circuit (as represented by the network 2 interface circuit 124). The basic structure of the assembly 100 may be found in the specification on page 5, lines 5-16 and is illustrated in FIG. 2. The first circuit 122 may be configured to delineate a receive frame RX1 received from a first network 104 having a first network protocol to produce an incoming packet INP1. Operations of the first interface 122 are generally described in the specification on page 8, lines 14-18. Further details may be found on page 20, line 16 through page 21, line 13 as shown in FIG. 6.

The second circuit 126 may be configured to (i) store a plurality of pointer values for a plurality of first parameters defined by the first network protocol, wherein each one of the first parameters is associated with a corresponding one of the pointer values. The pointer values are generally represented by the signal POINTER in FIG. 2 and are described in the specification on page 12, lines 14-21. The pointer values may specify how the parameters received in an incoming packet INP1 from network 104 are to be processed (specification page 13, lines 10-11). An example of the relationships of the pointer values to parameters in an Ethernet frame is shown in FIG. 5 and

described in the text on page 18, lines 1-10. The second circuit 126 may also be configured to (ii) process a particular one of the first parameters in the incoming packet INP1 in accordance with the corresponding pointer value to produce a second parameter. Processing of a particular first parameter is generally described in the specification on page 14, line 1 through page 15, line 7. Details of the internal workings of the second circuit 126 are also shown in FIG. 3. Descriptions of the processing performed by the peripherals 132a-132q on the parameters may be found on page 14, line 8 through page 15, line 7. The second circuit 126 may be further configured to (iii) present an outgoing packet OUTP1 containing the second parameter. Assembly and presentation of the outgoing packet OUTP1 may be performed by the assembler 136, as described in the specification on page 15, lines 8-17.

The third circuit 124 may be configured to frame the outgoing packet OUTP1 to present a transmit frame TX2 to a second network 106. Operation of the third circuit 124 is generally described on page 10, lines 1-8 of the specification. Further details may be found on page 20, lines 3-15 as shown in FIG. 6.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The first issue is whether claims 1-6 and 8-17 are patentable under 35 U.S.C. §102(e) over Ogawa et al. (hereafter Ogawa), U.S. Patent No. 5,936,966.

The second issue is whether claim 7 is patentable under 35 U.S.C. §103(a) over Ogawa in view of Official Notice that providing at least two peripheral blocks from a group of peripheral blocks is well known in the art.

The third issue is whether claim 18 is patentable under 35 U.S.C. §103(a) over Ogawa in view of Gabrick et al. (hereafter Gabrick), U.S. Patent Publication No. 2002/0161802.

The fourth issue is whether claim 19 is patentable under 35 U.S.C. §103(a) over Ogawa and Gabrick in view of Wilford et al. (hereafter Wilford), U.S. Patent No. 6,687,247.

The fifth issue is whether claim 20 is patentable under 35 U.S.C. §103(a) over Ogawa in view of Yanagihara et al. (hereafter Yanagihara), U.S. Patent No. 5,899,578.

VII. ARGUMENTS

A. 35 U.S.C. § 102

The Federal Circuit has stated: "A claim is anticipated only if ***each and every element*** as set forth in the claim is found, either ***expressly or inherently*** described, in a single prior art reference."[1] "The elements must be ***arranged as required by the claim***."[2] The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[3]

1. Claim 1 is fully patentable over Ogawa

Claim 1 provides an assembly in the preamble. The Examiner alleges that the text in column 3, lines 44-49 and column 4, line 65 to column 5, line 22 of Ogawa describes an item similar to the claimed assembly.[4] Based on the cites provided, the Examiner appears to be asserting that a data receiving device 106 shown in FIGS. 1, 26 and 27 of Ogawa is similar to the claimed assembly.

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[1] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Rev. 5, August 2006, §2131 citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Circ. 1987) (emphasis added).

[2] M.P.E.P. §2131 citing *In re Bond,* 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990) (emphasis added).

[3] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[4] Final Office Action, August 31, 2006, page 8, item 10.

Claim 1 further provides a database circuit configured to store a plurality of pointer values, wherein each one of the first parameters is associated with a corresponding one of the pointer values. Despite the assertion by the Examiner[5], the text in column 6, lines 38-67 of Ogawa is silent regarding a database circuit in the data receiving device 106 (alleged claimed assembly):

> FIG. 28 is a flowchart showing a sequence of the repeating operation when the repeater is a bridge;
> FIG. 29 is a flowchart showing a sequence of the repeating operation when the repeater is a router; and
> FIG. 30 is a flowchart showing a sequence of the repeating operation when the repeater is a router having to a firewall function.
>
> DESCRIPTION OF THE PREFERRED EMBODIMENTS
>
> Preferred embodiments according to the present invention will now be described in detail hereunder with reference to the accompanying drawings.
> FIG. 1 is a block diagram showing the structure of a data receiving device of a first embodiment to which the present invention is applied.
> As shown in FIG. 1, the first embodiment basically comprises: an input data control circuit 22; a capture register circuit 24; a protocol recognition circuit 26; a sequence selection circuit 28; a sequence counter 30; a sequencer 32; and a header end timing detection circuit 36. The present invention further comprises a frame end detection circuit 34 and an interrupt generation circuit 38 in this embodiment, but the invention is not restricted to this structure for application. Various modes of the above-mentioned components can be considered, and a first cut-through circuit 23 may be provided to an output side of a pipeline register (which will be simply referred to as a pipeline hereunder) constituting the input data control circuit 22 as shown in ...

Nowhere in the above text, or in any other section does Ogawa explicitly or inherently disclose a database circuit, a plurality of pointer values and an association of each one of the first parameters of an incoming packet to a corresponding one of the pointer values as required by M.P.E.P. §2131. In contrast, FIG. 1 of Ogawa discloses that the data receiving device 106 has an input data control circuit 22, a capture register circuit 24, a protocol recognition circuit 26, a sequence selection circuit 28, a sequence counter 30, a sequencer 32, a frame end detection circuit 34, a header end timing detection circuit 36, an interrupt generation circuit 38 and an external circuit 40. The data receiving device 106 of Ogawa has a structure that does not include anything that one of ordinary skill in the art would consider similar to the claimed database circuit as required by *Scripps Clinic & Research*

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[5] Final Office Action, August 31, 2006, page 9, top paragraph.

Found. Therefore, Ogawa does not disclose or suggest a database circuit configured to store a plurality of pointer values, wherein each one of the first parameters is associated with a corresponding one of the pointer values as presently claimed.

Furthermore, the rejection of claim 1 is based on language different than as claimed. The Examiner improperly changed the wording of the claim from the phrase "each one" to the phrase "only one".[6] Webster's New Collegiate Dictionary, copyright 1979, defines "each one" as a pronoun of "each". The word "each" is defined as "being one of two or more distinct individuals having a similar relation and often constituting an aggregate." The word "only" is defined as "a single fact or instance and nothing more or different." Hence, the phrases "each one" and "only one" have very different meanings. In contrast, no evidence is on record to support the Examiner's position that the phrases are synonymous. Therefore, one of ordinary skill in the art would not consider the phrase "each one" to mean "only one" as alleged by the Examiner. As such, the rejection of claim 1 does not consider the plain meaning of the actual claim language and the rejection cannot be sustained.

Claim 1 further provides a processing circuit configured to (i) process a particular one of the first parameters in an incoming packet received by the assembly in accordance with the corresponding pointer value to produce a second parameter and (ii) present an outgoing packet from the assembly containing the second parameter. Despite the assertion by the Examiner[7], the text in column 13, lines 26-55 of Ogawa is silent regarding a processing circuit in the data receiving device 106 (alleged claimed assembly):

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[6] Final Office Action, August 31, 2006, page 9, top paragraph.

[7] Final Office Action, August 31, 2006, page 9, second paragraph.

source network address; and the IP protocol information IP7, a destination network address. The IP protocol information IP8 is an optional field whose existence or length can be arbitrarily set.

TCP header data TCPH received in synchronism with WR20 to WR31 has TCP protocol information TC1 to TC9. The TCP protocol information TC1 indicates a receive port of the internetwork repeater using the data receiving device according this embodiment and the TCP protocol information TC2 indicates a transmit port. The TCP protocol information TC3 indicates a serial number of the received frame data. Further, TCP transmit data TCPD following the TCP header data TCPH is received. These TCP header data TCPH and the TCP transmit data TCPD are based on the TCP protocol.

Here, those based on the TCP protocol can be substituted by those based on the ICMP protocol or the UDP protocol.

Note that the IP protocol information IP1 is made up of parameters of Version (four bits), IHL (header length consisting of four bits) and TOS (type of service consisting of eight bits). Further, the IP protocol information IP4 is constituted by TTL (time to live, eight bits) and a protocol code representing a protocol of the transport layer. Incidentally, the TCP protocol information TC4 indicates an acknowledge number; the TCP protocol information TC5, an offset/flag; the TCP protocol information TC6, a window; the TCP protocol information TC8, an object pointer; and the TCP protocol information TC9, an optional field.

Nowhere in the above text, or in any other section does Ogawa explicitly or inherently disclose a processing circuit, a particular one of the first parameters, the corresponding pointer value, a second parameter and an outgoing packet as required by M.P.E.P. §2131. In contrast, FIGS. 1, 26 and 27 of Ogawa show that the data receiving device 106 does not present any outgoing packet, particularly no outgoing packet having a second parameter based on a first parameter in an incoming packet. The data receiving device 106 of Ogawa (alleged claimed assembly) has a structure that does not include anything that one of ordinary skill in the art would consider similar to the claimed processing circuit as required by *Scripps Clinic & Research Found.* Therefore, Ogawa does not disclose or suggest a processing circuit configured to (i) process a particular one of the first parameters in an incoming packet received by the assembly in accordance with the corresponding pointer value to produce a second parameter and (ii) present an outgoing packet from the assembly containing the second parameter as presently claimed.

In summary, Ogawa does not disclose the claimed structure as required by M.P.E.P. §2131. The structure of Ogawa does not include anything that one of ordinary skill in the art would consider to be similar to the claimed database circuit and the claimed processing circuit. Ogawa also

lacks any element similar to the claimed pointer values. As such, claim 1 is fully patentable over the cited reference. Furthermore, the rejections provide little more than lists of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. In addition, the rejection fails to account for the plain language of the claim by replacing the phrase "each one" with the phrase "only one". Therefore, *prima facie* anticipation has not been established and rejection should with reversed.

2. Claims 10 and 12 are fully patentable over Ogawa

Claim 10 provides an assembly in the preamble. The Examiner alleges that the text in column 3, lines 44-49 and column 4, line 65 to column 5, line 22 of Ogawa describes an item similar to the claimed assembly.[8] Based on the cites provided, the Examiner appears to be asserting that a data receiving device 106 shown in FIGS. 1, 26 and 27 of Ogawa is similar to the claimed assembly.

Claim 10 further provides a first circuit configured to delineate a receive frame received from a first network having a first network protocol to produce an incoming packet. Despite the assertion by the Examiner[9], the text in column 12, lines 41-49 and column 2, lines 5-14 of Ogawa is silent regarding a circuit in the data receiving device 106 (alleged claimed assembly) configured to delineate a receive frame from a network:

> If the present embodiment is used in the internetwork repeater and the transmission operation is started in the external computer using the interrupt signal IPS indicating the end timing for the header, the process is enabled with relay of the frame data rarely delayed. Additionally, if the present embodiment is used in the internetwork repeater and the

[8] Final Office Action, August 31, 2006, page 8, item 10.

[9] Final Office Action, August 31, 2006, page 9, third paragraph.

transmission operation for relaying the received frame data is started by the ID of the end timing for the frame data, the highly-reliable relay operation is enabled. (Col. 12 lines 41-49)

...

Here, an internetwork repeater by which two networks having the same MAC (Media Access Control) layer in the second layer of OSI are connected in the second layer is called a bridge or the like. An internetwork repeater for connecting a plurality of networks having different first through seventh layers of OSI is called a gateway or the like. Further, an internetwork repeater for connecting a plurality of networks having different first to third layers of OSI, are connected in the third layer such as one described later in this specification is called a router or the like. (Col. 2 lines 5-14)

Nowhere in the above text, or in any other section does Ogawa expressly or inherently disclose a first circuit configured to delineate a receive frame to produce an incoming packet as required by M.P.E.P. §2131. In contrast, column 20, lines 18-51 of Ogawa states that a data frame received through an input port 102 is stored in a memory 112, processed, then transmitted as a modified data frame through an output port 104. Nowhere in Ogawa is the data frame delineated to produce an incoming packet. Furthermore, none of the input port 102, the memory 112 and the output port 104 of Ogawa are part of the data receiving device 106 (alleged claimed assembly). Therefore, Ogawa does not disclose or suggest a first circuit configured to delineate a receive frame received from a first network having a first network protocol to produce an incoming packet as presently claimed.

Claim 10 further provides a second circuit configured to (i) store a plurality of pointer values for a plurality of first parameters defined by the first network protocol, wherein each one of the first parameters is associated with a corresponding one of the pointer values, (ii) process a particular one of the first parameters in the incoming packet in accordance with the corresponding pointer value to produce a second parameter, and (iii) present an outgoing packet containing the second parameter. Despite the assertion by the Examiner[10], the text in column 12, lines 41-49 and

[10] Final Office Action, August 31, 2006, page 9, bottom paragraph.

column 2, lines 5-14 of Ogawa is silent regarding a second circuit in the data receiving device 106 (alleged claimed assembly) that stores pointers, processes parameters and produces outgoing packets:

> If the present embodiment is used in the internetwork repeater and the transmission operation is started in the external computer using the interrupt signal IPS indicating the end timing for the header, the process is enabled with relay of the frame data rarely delayed. Additionally, if the present embodiment is used in the internetwork repeater and the transmission operation for relaying the received frame data is started by the ID of the end timing for the frame data, the highly-reliable relay operation is enabled. (Col. 12 lines 41-49)
>
> ...
>
> Here, an internetwork repeater by which two networks having the same MAC (Media Access Control) layer in the second layer of OSI are connected in the second layer is called a bridge or the like. An internetwork repeater for connecting a plurality of networks having different first through seventh layers of OSI is called a gateway or the like. Further, an internetwork repeater for connecting a plurality of networks having different first to third layers of OSI, are connected in the third layer such as one described later in this specification is called a router or the like. (Col. 2 lines 5-14)

Nowhere in the above text, or in any other section does Ogawa expressly or inherently disclose a second circuit configured to (i) store a plurality of pointer values for a plurality of first parameters defined by the first network protocol, wherein each one of the first parameters is associated with a corresponding one of the pointer values, (ii) process a particular one of the first parameters in the incoming packet in accordance with the corresponding pointer value to produce a second parameter, and (iii) present an outgoing packet containing the second parameter as required by M.P.E.P. §2131. In contrast, FIGS. 1, 26 and 27 of Ogawa do not show any output from the data receiving device 106 (alleged claimed assembly) that could be considered to be an outgoing packet. Therefore, Ogawa does not disclose or suggest a second circuit configured to (i) store a plurality of pointer values for a plurality of first parameters defined by the first network protocol, wherein each one of the first parameters is associated with a corresponding one of the pointer values, (ii) process a particular one of the first parameters in the incoming packet in accordance with the corresponding pointer value to produce a second parameter, and (iii) present an outgoing packet containing the second parameter as presently claimed.

Furthermore, the rejection of claim 10 is based on language different than as claimed. The Examiner improperly changed the wording of the claim from the phrase "each one" to the phrase "only one".[11] Webster's New Collegiate Dictionary, copyright 1979, defines "each one" as a pronoun of "each". The word "each" is defined as "being one of two or more distinct individuals having a similar relation and often constituting an aggregate." The word "only" is defined as "a single fact or instance and nothing more or different." Hence, the phrases "each one" and "only one" have very different meanings. In contrast, no evidence is on record to support the Examiner's position that the phrases are synonymous. Therefore, one of ordinary skill in the art would not consider the phrase "each one" to mean "only one" as alleged by the Examiner. As such, the rejection of claim 10 does not consider the plain meaning of the actual claim language and the rejection cannot be sustained.

Claim 10 further provides a third circuit configured to frame the outgoing packet to present a transmit frame to a second network. Despite the assertion by the Examiner[12], the text in column 12, lines 41-49 and column 2, lines 5-14 of Ogawa is silent regarding a third circuit in the data receiving device 106 (alleged claimed assembly) configured to frame outgoing packets:

> If the present embodiment is used in the internetwork repeater and the transmission operation is started in the external computer using the interrupt signal IPS indicating the end timing for the header, the process is enabled with relay of the frame data rarely delayed. Additionally, if the present embodiment is used in the internetwork repeater and the transmission operation for relaying the received frame data is started by the ID of the end timing for the frame data, the highly-reliable relay operation is enabled. (Col. 12 lines 41-49)
> ...
>
> Here, an internetwork repeater by which two networks having the same MAC (Media Access Control) layer in the second layer of OSI are connected in the second layer is called a bridge or the like. An internetwork repeater for connecting a plurality of networks having different first through seventh layers of OSI is called a gateway or the like. Further, an internetwork repeater for connecting a plurality of networks having different first to third layers of OSI, are connected in the third layer such as one described later in this specification is called a router or the like. (Col. 2 lines 5-

[11] Final Office Action, August 31, 2006, page 9, top paragraph.

[12] Final Office Action, August 31, 2006, page 10, top paragraph.

14)

Nowhere in the above text, or in any other section does Ogawa expressly or inherently disclose a third circuit configured to frame the outgoing packet to present a transmit frame to a second network as required by M.P.E.P. §2131. In contrast, FIG. 27 of Ogawa shows that there is no connection between the data receiving device 106 (alleged claimed assembly) and a network connected to one of the output ports 104. Furthermore, column 20, lines 45-51 of Ogawa state that the output ports 104 receive data frames (not packets to be encapsulated by the data frames) from the memory 112. Therefore , Ogawa does not disclose or suggest a third circuit configured to frame the outgoing packet to present a transmit frame to a second network as presently claimed.

In summary, Ogawa does not expressly or inherently disclose the claimed structure as required by M.P.E.P. §2131. The structure of Ogawa does not include anything that one of ordinary skill in the art would consider to be similar to the claimed first circuit, the claimed second circuit and the claimed third circuit. Ogawa also lacks any element similar to the claimed pointer values. As such, claim 10 is fully patentable over the cited reference. Furthermore, the rejections provide little more than lists of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. In addition, the rejection fails to account for the plain language of the claim by replacing the phrase "each one" with the phrase "only one". As such, *prima facie* anticipation has not been established and rejection of claims 10 and 12 should with reversed.

3. Claims 2 and 11 are fully patentable over Ogawa

Claim 2 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 2. Claim 11 depends from claim 10 and thus contains all of the limitations of claim 10. Consequently, the arguments presented above in support of the patentability of claim 10 are incorporated hereunder in support of claim 11.

Claim 2 further provides that (i) the database circuit is further configured to store a plurality of offset values and a plurality of length values for the first parameters, each one of the first parameters is further associated with both a corresponding one of the offset values and a corresponding one of the length values and (ii) the processing circuit is further configured to partition the incoming packet in accordance with at least one of the offset values and at least one of the length values to extract the particular first parameter. In contrast, Ogawa is silent and the Examiner has not identified any elements of Ogawa that one of ordinary skill in the art would consider to be similar to the claimed database circuit and the claimed processing circuit. Furthermore, the cites into Ogawa provided in the rejection of claim 2 do not place offset values and length values in anything that could be considered similar to the claimed database circuit. The cites into Ogawa do not disclose any processing per the alleged offset values and the alleged length values. The rejections provided by the Examiner are little more than lists of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that (i) the database circuit is further configured to store a plurality of offset values and a plurality of length values for the first parameters,

each one of the first parameters is further associated with both a corresponding one of the offset values and a corresponding one of the length values and (ii) the processing circuit is further configured to partition the incoming packet in accordance with at least one of the offset values and at least one of the length values to extract the particular first parameter as presently claimed. As such, claims 2 and 11 are fully patentable over the cited reference and the rejection should be reversed.

4. Claim 3 is fully patentable over Ogawa

Claim 3 depends from claim 2 and thus contains all of the limitations of claim 2. Consequently, the arguments presented above in support of the patentability of claim 2 are incorporated hereunder in support of claim 3.

Claim 3 further provides that the assembly further comprises an interface through which the offset values, the length values and the pointer values are downloaded for storage in the database circuit. Despite the assertion by the Examiner[13], the text in column 11, lines 58-67 and column 13, lines 15-21 of Ogawa is silent regarding an interface of the data receiving device 106 (alleged claimed assembly) having an interface to some unidentified alleged database circuit to download unidentified alleged offset values, length values and pointer values. The rejection provides little more than a list of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that the assembly further comprises an interface through which the offset values,

[13] Final Office Action, August 31, 2006, page 10, item 12.

the length values and the pointer values are downloaded for storage in the database circuit as presently claimed. As such, claim 3 is fully patentable over the cited reference and the rejection should be reversed.

5. Claims 4 and 6 are fully patentable over Ogawa

Claim 4 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 4.

Claim 4 further provides that the processing circuit comprises (A) a parsing circuit configured to partition the incoming packet, (B) a plurality of peripheral blocks (i) coupled to the parsing circuit, (ii) identified by the pointer values and (iii) configured to perform a plurality of processes involving the first parameters and (C) an assembling circuit coupled to the peripheral blocks and configured to generate the outgoing packet. In contrast, Ogawa is silent and the Examiner has not identified any element of Ogawa that one of ordinary skill in the art would consider to be similar to the claimed processing circuit. Furthermore, the rejection does not place the various cited elements of Ogawa within the unidentified alleged processing circuit. The rejection provides little more than a list of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that the processing circuit comprises (A) a parsing circuit configured to partition the incoming packet, (B) a plurality of peripheral blocks (i) coupled to the parsing circuit, (ii) identified by the pointer values and (iii) configured to perform a plurality of processes involving the

first parameters and (C) an assembling circuit coupled to the peripheral blocks and configured to generate the outgoing packet as presently claimed. As such, claims 4 and 6 are fully patentable over the cited reference and the rejection should be reversed.

6. Claim 5 is fully patentable over Ogawa

Claim 5 depends from claim 4 and thus contains all of the limitations of claim 4. Consequently, the arguments presented above in support of the patentability of claim 4 are incorporated hereunder in support of claim 5.

Claim 5 further provides that the database circuit is further configured to store both a second offset value and a second length value for the second parameter as defined by a second network protocol. Despite the assertion by the Examiner[14], the text in column 3, lines 1-23 of Ogawa is silent regarding offset values and length values of a parameter defined by a second network protocol:

> The above processes are carried out in accordance with each protocol hierarchy of the received frame data and definition of each protocol hierarchy. Therefore, processes to be performed differ depending on each protocol and each protocol hierarchy constituting the protocol. Some protocol hierarchies may have a header containing an optional field whose existence or length is indefinite and, in such a case, processes for the header may differ depending on each protocol hierarchy because the header length is not fixed even in the same protocol hierarchy. Thus, in the prior art, processes for the frame data received by the data receiving device have been generally carried out using flexible software.
>
> However, the operation for advancing such processes executed in the data receiving device starting from the lower protocol hierarchy, i.e., the physical layer while confirming the protocol information (parameters) in each header has a large throughput and requires large CPU (Central Processing Unit) power, bottlenecking the processes in the data receiving device. Since the property of real time is basically required for the processes executed in the data receiving device, such problems are becoming serious as the processing speed in a target network is increased. For example, in case of the internetwork repeater determining a recent network having a high processing speed as a target in particular, if the process for linking one network to another network is delayed, the communication speed inherent to the network itself is decreased and the high processing speed can not be fully used, resulting in the drawback which must be urgently solved.

[14] Final Office Action, August 31, 2006, page 11, item 14.

Nowhere in the above text, or in any other section does Ogawa expressly or inherently disclose storing offset values and length values as required by M.P.E.P. §2131. The rejection provides little more than a list of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that the database circuit is further configured to store both a second offset value and a second length value for the second parameter as defined by a second network protocol as presently claimed. As such, claim 5 is fully patentable over the cited reference and the rejection should be reversed.

7. Claim 8 is fully patentable over Ogawa

Claim 8 depends from claim 4 and thus contains all of the limitations of claim 4. Consequently, the arguments presented above in support of the patentability of claim 4 are incorporated hereunder in support of claim 8.

Claim 8 further provides that the peripheral blocks are configured to simultaneously processes a plurality of the first parameters. Despite the assertion by the Examiner[15], the text in column 6, lines 1-15 of Ogawa is silent regarding multiple peripheral circuits processing multiple first parameters simultaneously:

> FIG. 9 is a timing chart continued from FIG. 8;
> FIG. 10 is a timing chart continued from FIG. 9;
> FIG. 11 is a flowchart showing an example of the retrieval operation executed by the second cut-through circuit in a router;
> FIG. I2 is a timing chart showing the operation of the first embodiment when frame data of DIX-IP-TCP is received;
> FIG. I3 is a timing chart continued from FIG. I2;
> FIG. 14 is a timing chart continued from FIG. 13;
> FIG. I5 is a timing chart continued from FIG. 14;
> FIG. 16 is a timing chart showing the operation of the first embodiment when frame data of DIX-IPX-SPX is received;
> FIG. I7 is a timing chart continued from FIG. 16;
> FIG. 18 is a timing chart continued from FIG. 17;

[15] Final Office Action, August 31, 2006, page 11, item 16.

FIG. 19 is a timing chart continued from FIG. 18;

Nowhere in the above text, or in any other section does Ogawa explicitly or inherently disclose that a plurality of peripheral blocks are configured to simultaneously processes a plurality of the first parameters as required by M.P.E.P. §2131. As such, claim 8 is fully patentable over the cited reference and the rejection should be reversed.

8. Claim 9 is fully patentable over Ogawa

Claim 9 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 9.

Claim 9 further provides that the processing circuit is implemented as only hardware. Despite the assertion by the Examiner[16], the text in column 5, lines 8-38, column 1, lines 41-43 and column 5, lines 43-45 of Ogawa is silent regarding hardware only processing circuits:

> (X-series recommendations) relative to new data networks such as a line switching system, a packet switching system, digital private lines and others. (Column 1, lines 41-43)
> ...
> Furthermore, when source/destination addresses, port numbers, socket numbers or protocol codes included in the headers of a plurality of protocol hierarchies are combined to create key data for retrieval and table retrieval is executed, the process required for the V-LAN (Virtual LAN) or the so-called "Firewall" to enhance security by restricting access to information can be executed at extremely-high speed, as well as the process in the bridge or the router.
> n addition, if there is provided a cut-through selection circuit for selecting and outputting one of signals output from the first cut-through circuit and the second cut-through circuit, a cut-through system can be selected.
> Further, if the input data control circuit has a configuration for taking out a destination address from the header in the protocol hierarchy for the received data and transmitting it to an external circuit, it is possible to readily cope with a multi-protocol system.
> Furthermore, if information stored and/or held in the capture register circuit or a protocol of each protocol hierarchy identified by the protocol recognition circuit can be read out to an external circuit, various functions can be realized.
> Moreover, if the input data control circuit has a function for verifying a checksum with respect to the received data frame and a function for transmitting a result of verification to an external circuit and the sequencer has a function for directing a timing at which the checksum operation is started and a timing at which results of the checksum operation are compared with each other to the input data control circuit, data can be verified with the simple configuration.

[16] Final Office Action, August 31, 2006, page 12, item 17.

> According to the present invention, processes for a plurality of protocol hierarchies for defining a protocol for the received frame data or partial processes thereof can be simply and efficiently carried out at the same time. Additionally, the data receiving device for effecting these processes can be easily and comprehensively constructed using the hardware. (Column 5, lines 7-45)

Nowhere in the above text, or in any other sections does Ogawa explicitly or inherently disclose some unidentified alleged processing circuit that is implemented as only hardware as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that the processing circuit is implemented as only hardware as presently claimed. As such, claim 9 is fully patentable over the cited reference and the rejection should be reversed.

9. Claim 13 is fully patentable over Ogawa

Claim 13 depends from claim 10 and thus contains all of the limitations of claim 10. Consequently, the arguments presented above in support of the patentability of claim 10 are incorporated hereunder in support of claim 13.

Claim 13 further provides that the assembly further comprises an interface configured to permit a selection among a plurality of frame delineation methods. Despite the assertion by the Examiner[17], the text in column 5, lines 41-57 and column 8, line 58 through column 9, line 24 of Ogawa is silent regarding an interface of the data receiving device 106 (alleged claimed assembly) used for selecting frame delineation methods. The rejection provides little more than a list of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that the assembly, further comprises an interface configured to permit a selection among a plurality of frame delineation

[17] Final Office Action, August 31, 2006, page 12, item 20.

methods as presently claimed. As such, claim 13 is fully patentable over the cited reference and the rejection should be reversed.

10. Claim 14 is fully patentable over Ogawa

Claim 14 depends from claim 10 and thus contains all of the limitations of claim 10. Consequently, the arguments presented above in support of the patentability of claim 10 are incorporated hereunder in support of claim 14.

Claim 14 further provides that the third circuit is further configured to provided a plurality of framing methods for a plurality of network protocols. Despite the assertion by the Examiner[18], the text in column 4, lines 4-57, column 6, line 62 through column 7, line 24 and column 8, lines 54-56 of Ogawa is silent regarding a plurality of framing methods. Furthermore, the rejection provides little more than a list of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that the third circuit is further configured to provided a plurality of framing methods for a plurality of network protocols as presently claimed. As such, claim 14 is fully patentable over the cited reference and the rejection should be reversed.

[18] Final Office Action, August 31, 2006, page 13, item 21.

11. Claim 15 is fully patentable over Ogawa

Claim 15 depends from claim 14 and thus contains all of the limitations of claim 14. Consequently, the arguments presented above in support of the patentability of claim 14 are incorporated hereunder in support of claim 15.

Claim 15 further provides that the assembly, further comprises an interface configured to permit a selection among the framing methods. Despite the assertion by the Examiner[19], the text in column 3, lines 41-57 column 8, line 58 through column 9, line 24 and figure 11 of Ogawa is silent regarding an interface of the data receiving device 106 (alleged claimed assembly) used for selecting framing methods. The rejection provides little more than a list of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that the assembly, further comprises an interface configured to permit a selection among the framing methods as presently claimed. As such, claim 15 is fully patentable over the cited reference and the rejection should be reversed.

12. Claim 16 is fully patentable over Ogawa

Claim 16 depends from claim 10 and thus contains all of the limitations of claim 10. Consequently, the arguments presented above in support of the patentability of claim 10 are incorporated hereunder in support of claim 16.

Claim 16 further provides that the third circuit is further configured to delineate a second receive frame from the second network to produce a second incoming packet. Despite the

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[19] Final Office Action, August 31, 2006, page 12, item 22.

assertion by the Examiner[20], the text in column 3, lines 41-57, figures 11 and 15 and column 8, line 58 through column 9, line 24 of Ogawa is silent regarding some unidentified alleged third circuit delineating a received frame to produce an incoming frame. In contrast, FIG. 27 of Ogawa shows that the input port 102 for receiving data frames is separated from the output port 104 for transmitting data frames. Furthermore, the rejection provides little more than a list of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that the third circuit is further configured to delineate a second receive frame from the second network to produce a second incoming packet as presently claimed. As such, claim 16 is fully patentable over the cited reference and the rejection should be reversed.

13. Claim 17 is fully patentable over Ogawa

Claim 17 depends from claim 16 and thus contains all of the limitations of claim 16. Consequently, the arguments presented above in support of the patentability of claim 16 are incorporated hereunder in support of claim 17.

Claim 17 further provides that the first circuit is further configured to frame a second outgoing packet derived from the second incoming packet to present a second transmit frame to the first network. Despite the assertion by the Examiner[21], the text in column 5, lines 41-57, column 3, lines 51-67, column 4, line 50 through column 5, line 14 and column 6, line 62 through column 7,

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[20] Final Office Action, August 31, 2006, page 13, item 23.

[21] Final Office Action, August 31, 2006, page 13, item 24.

line 24 of Ogawa is silent regarding some unidentified alleged first circuit framing a packet to produce an outgoing frame. In contrast, FIG. 27 of Ogawa shows that the input port 102 for receiving data frames is separated from the output port 104 for transmitting data frames. Furthermore, the rejection provides little more than a list of columns and lines in Ogawa that do not tie the various elements of Ogawa together per the claims as required by M.P.E.P. §2131. Therefore, Ogawa does not disclose or suggest that the first circuit is further configured to frame a second outgoing packet derived from the second incoming packet to present a second transmit frame to the first network as presently claimed. As such, claim 17 is fully patentable over the cited reference and the rejection should be reversed.

B **35 U.S.C. § 103**

The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness.[22] If the Examiner does not produce a *prima facie* case, the Applicant is under no obligation to submit evidence of non-obviousness.[23] ***The Examiner must show*** that (a) there is some ***suggestion or motivation***, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is ***a reasonable expectation of success***, and (c) the prior art reference (or combination of references) teaches or suggests ***all of the claim limitations***.[24] "The motivation, suggestion or teaching may come

[22] M.P.E.P §2142.

[23] M.P.E.P. §2142.

[24] M.P.E.P. §2142.

explicitly from statement in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved."[25] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "***rigorous***" and must be "***clear and particular***".[26] "[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of ***making the specific combination that was made by the applicants.***"[27] "[T]he factual inquiry whether to combine references must be ***thorough and searching***."[28] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[29] "It must be ***based on objective evidence of record***."[30] The Federal Circuit has held that both the suggestion to modify or combine the references and the reasonable expectation success must be found in the prior art itself, not merely in Appellant's disclosure.[31] Furthermore, the Board has held that the claimed invention is obvious only if either the references expressly or implicitly suggest the claimed invention, or a convincing line of reasoning is presented by the examiner as to why an

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[25] *In re Huston* 308, F.3d 1267, 1278, 64 USPQ2d 1810, 1810 (Fed. Cir. 2002), citing *In re Katzab* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000)

[26] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

[27] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[28] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[29] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[30] *In re Lee* at 1343, 61 USPQ2d at 1434.

[31] *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991).

artisan would have found the claimed invention to be obvious in light of the teachings of the cited references.[32]

1. Claim 7 is fully patentable over Ogawa and Official Notice

Claim 7 depends from claim 4 and thus contains all of the limitations of claim 4. Consequently, the arguments presented above in support of the patentability of claim 4 are incorporated hereunder in support of claim 7.

Regarding claim 7, the proposed motivations to modify Ogawa with the Official Notice are improperly based on the claim. The proposed motivations, (i) "support handling of the packet related information" and (ii) "help processing information that is related to the packets" are too general because they could cover almost any alteration contemplated and do not address why the specific proposed modification would have been obvious. Broad conclusory statements regarding the obviousness of combining/modifying references, standing alone, are not "evidence" as required by M.P.E.P. §2142. Furthermore, no evidence is on record identifying the sources of the alleged motivations. Therefore, *prima facie* obviousness has not been established for lack of evidence on the record for appropriate motivation to modify Ogawa. As such, the rejection of claim 7 should be reversed for lack of evidence of motivation to modify the reference.

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[32] See *Ex Parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985) (emphasis added by Appellant).

2. Claim 18 is fully patentable over Ogawa and Gabrick

Claim 18 depends from claim 10 and thus contains all of the limitations of claim 10. Consequently, the arguments presented above in support of the patentability of claim 10 are incorporated hereunder in support of claim 18.

Claim 18 further provides that the first circuit comprises a plurality of framing circuits configured to operate on a plurality of network protocols, wherein each one of the framing circuits operates on a corresponding one of the network protocols. Despite the assertion by the Examiner[33], the text in column 3, lines 44-66 of Ogawa is silent regarding multiple framing circuits. In contrast, the data receiving device 106 of Ogawa (alleged claimed assembly) does not perform any framing operations. Therefore, Ogawa and Gabrick, alone or in combination, do not teach or suggest that the first circuit comprises a plurality of framing circuits configured to operate on a plurality of network protocols, wherein each one of the framing circuits operates on a corresponding one of the network protocols as presently claimed.

Furthermore, the proposed motivation to modify Ogawa with the Gabrick is improperly based on the claim. The proposed motivation, "support replicating and transferring information between two entities" is too general because it could cover almost any alteration contemplated and does not address why the specific proposed modification would have been obvious. A broad conclusory statement regarding the obviousness of combining/modifying references, standing alone, is not "evidence" as required by M.P.E.P. §2142. Furthermore, no evidence is on record identifying the source of the alleged motivation. Therefore, *prima facie*

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[33] Final Office Action, August 31, 2006, page 15, item 28.

obviousness has not been established due to a lack of evidence of motivation to combine/modify Ogawa and Gabrick.

Furthermore, Gabrick is non-analogous art relative to Ogawa based on the respective U.S. classifications. Gabrick appears to have been selected only because it contains the claim phrase "unique network protocol", not because one of ordinary skill in the art would have considered it to be analogous art. There is no evidence on record to support the Examiner's position that the references would be considered analogous. Therefore, *prima facie* obviousness has not been established. As such, claim 18 is fully patentable over the cited references and the rejection should be reversed.

3. Claim 19 is fully patentable over Ogawa , Wilford and Gabrick

Claim 19 depends from claim 10 and thus contains all of the limitations of claim 10. Consequently, the arguments presented above in support of the patentability of claim 10 are incorporated hereunder in support of claim 19.

Claim 19 further provides that the third circuit comprises a plurality of de-framing circuits configured to operate on a plurality of network protocols, wherein each one of the de-framing circuits operates on a corresponding one of the network protocols. Despite the assertion by the Examiner[34], the text in column 2, line 59 to column 3, line 18 of Ogawa is silent regarding multiple de-framing circuits. In contrast, Ogawa is silent regarding the data receiving device 106 (alleged claimed assembly) having even a single de-framing capability. For example, column 20, lines 18-51

[34] Final Office Action, August 31, 2006, page 16, item 30.

of Ogawa state that a data frame received by an input port 102 is stored as a frame in the memory 112 and then transmitted through an output port 104. Therefore, Ogawa, Wilford and Gabrick, alone or in combination, do not teach or suggest that the third circuit comprises a plurality of de-framing circuits configured to operate on a plurality of network protocols, wherein each one of the de-framing circuits operates on a corresponding one of the network protocols as presently claimed.

Furthermore, the proposed motivations to modify Ogawa and Gabrick with Wilford are improperly based on the claim. The proposed motivations, (i) "enhance the handling the information associated with the packet" and (ii) "help enhance the software to process information for the assembly" are too general because they could cover almost any alteration contemplated and does not address why the specific proposed modification would have been obvious. Broad conclusory statements regarding the obviousness of combining/modifying references, standing alone, are not "evidence" as required by M.P.E.P. §2142. Furthermore, no evidence is on record identifying the sources of the alleged motivations. Therefore, *prima facie* obviousness has not been established for lack of evidence of motivation to combine/modify the references.

Furthermore, Gabrick is non-analogous art relative to Ogawa and Wilford based on the respective U.S. classifications. Gabrick appears to have been selected only because it contains the claim phrase "unique network protocol", not because one of ordinary skill in the art would have found it to be analogous art. There is no evidence on record to support the Examiner's position that the references would be considered analogous. Therefore, *prima facie* obviousness has not been established. As such, claim 19 is fully patentable over the cited references and the rejection should be reversed.

4. Claim 20 is fully patentable over Ogawa and Yanagihara

Claim 20 depends from claim 10 and thus contains all of the limitations of claim 10. Consequently, the arguments presented above in support of the patentability of claim 10 are incorporated hereunder in support of claim 20.

Claim 20 further provides a fourth circuit connected to the second circuit and configured process a select one of the first parameters in the incoming packet in accordance with the corresponding pointer value. The Examiner merely states[35] that the claimed fourth circuit is taught by Yanagihara in FIG. 10A and column 1, lines 51-66:

> This invention aims to make it possible to perform rapid decoding of video data and audio data in a receiver/demodulator if there is a program change when a DVCR of the aforesaid type continuously plays back a plurality of digital broadcast programs, and this data is then input to such a receiver/demodulator.
> This invention further aims to provide a digital signal recording/playback device and digital signal playback method wherein there is no break in video data and audio data when the output during speed change playback of such a DVCR is input to a receiver/demodulator and decoded.
> To resolve the above problems, the digital signal processor according to this invention is characterized in comprising **first means for selecting a transport stream corresponding to any channel from a transport stream** containing a plurality of multiplexed channels, **second means for separating video data** and audio data in any desired program ... (Column 1, lines 51-66)(Emphasis added)

The Examiner appears to be arguing that the first means and the second means of Yanagihara somehow teach or suggest the claimed second circuit and the claimed fourth circuit. However, nowhere in the above text, or in any other section does Yanagihara mention that either the first means or the second means (alleged claimed fourth circuit) is configured to process a selected one of the first parameters (not identified in Yanagihara) in an incoming packet in accordance with the corresponding pointer values (not identified in Yanagihara). Since the pointer values and the first parameters are allegedly disclosed in Ogawa, one of ordinary skill in the art would not appear to understand how Yanagihara could use the pointer values from another document (or similar

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[35] Final Office Action, August 31, 2006, page 17, item 33.

unidentified pointer values within Yanagihara) to process and first parameters from the other document (or similar unidentified first parameters within Yanagihara). Therefore, Ogawa and Yanagihara, alone or in combination, do not teach or suggest a fourth circuit connected to a second circuit and configured process at least one of the first parameters in an incoming packet in accordance with a pointer as presently claimed.

Furthermore, the proposed motivations to modify Ogawa with Yanagihara are improperly based on the claim. The proposed motivations, (i) "another circuit would enhance the handling the information associated with the packet" and (ii) "help enhance the software to process information for the assembly" are too general because they could cover almost any alteration contemplated and does not address why the specific proposed modification would have been obvious. Broad conclusory statements regarding the obviousness of combining/modifying references, standing alone, are not "evidence" as required by M.P.E.P. §2142. Furthermore, no evidence is on record identifying the sources of the alleged motivations. Therefore, *prima facie* obviousness has not been established for lack of evidence of motivation to combine/modify the references. As such, claim 20 is fully patentable over the cited references and the rejection should be reversed.

C. CONCLUSION

None of the cited references suggest a circuit configured to store a plurality of pointer values for a plurality of parameters defined by a network protocol, wherein each one of the parameters is associated with a corresponding one of the pointer values, as recited in claims 1 and

10. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the claims are not rendered obvious by the cited reference. However, should the Board find the arguments herein in support of independent claims 1 and/or 10 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable claims.

Respectfully submitted,

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VIII. CLAIM APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. An assembly comprising:

a database circuit configured to store a plurality of pointer values for a plurality of first parameters defined by a network protocol, wherein each one of said first parameters is associated with a corresponding one of said pointer values; and

a processing circuit configured to (i) process a particular one of said first parameters in an incoming packet received by said assembly in accordance with said corresponding pointer value to produce a second parameter and (ii) present an outgoing packet from said assembly containing said second parameter.

2. The assembly according to claim 1, wherein (i) said database circuit is further configured to store a plurality of offset values and a plurality of length values for said first parameters, each one of said first parameters is further associated with both a corresponding one of said offset values and a corresponding one of said length values and (ii) said processing circuit is further configured to partition said incoming packet in accordance with at least one of said offset values and at least one of said length values to extract said particular first parameter.

3. The assembly according to claim 2, further comprising an interface through which said offset values, said length values and said pointer values are downloaded for storage in said database circuit.

4. The assembly according to claim 1, wherein said processing circuit comprises:

a parsing circuit configured to partition said incoming packet;

a plurality of peripheral blocks (i) coupled to said parsing circuit, (ii) identified by said pointer values and (iii) configured to perform a plurality of processes involving said first parameters; and

an assembling circuit coupled to said peripheral blocks and configured to generate said outgoing packet.

5. The assembly according to claim 4, wherein said database circuit is further configured to store both a second offset value and a second length value for said second parameter as defined by a second network protocol.

6. The assembly according to claim 4, further comprising an interface connectable to a peripheral block external to said assembly.

7. The assembly according to claim 4, wherein said peripheral blocks are at least two circuits selected from a group of circuits consisting of a content addressable memory circuit, a time to live circuit, a comparison circuit, a counter circuit, a value swapping circuit, a stuffing circuit, a de-stuffing circuit, a cyclic redundancy checksum circuit, a parity circuit, a first-in-first-out circuit, a length construction generator circuit, a header error control synchronization circuit, a frame

relay lookup circuit, a data link connection identifier circuit, a protocol identification analysis circuit, a point-to-point protocol verification circuit, a parameter discard circuit, and a buffer circuit.

8. The assembly according to claim 4, wherein said peripheral blocks are configured to simultaneously processes a plurality of said first parameters.

9. The assembly according to claim 1, wherein said processing circuit is implemented as only hardware.

10. An assembly comprising:

a first circuit configured to delineate a receive frame received from a first network having a first network protocol to produce an incoming packet;

a second circuit configured to (i) store a plurality of pointer values for a plurality of first parameters defined by said first network protocol, wherein each one of said first parameters is associated with a corresponding one of said pointer values, (ii) process a particular one of said first parameters in said incoming packet in accordance with said corresponding pointer value to produce a second parameter, and (iii) present an outgoing packet containing said second parameter; and

a third circuit configured to frame said outgoing packet to present a transmit frame to a second network.

11. The assembly according to claim 10, wherein said second circuit is further configured to (i) store a plurality of offset values and a plurality of length values for said first parameters, each one of said first parameters is further associated with both a corresponding one of said offset values and a corresponding one of said length values and (ii) partition said incoming packet in accordance with said offset values and said length values to extract said first parameters from said incoming packet.

12. The assembly according to claim 10, wherein said first circuit is further configured to provided a plurality of frame delineation methods for a plurality of network protocols.

13. The assembly according to claim 12, further comprising an interface configured to permit a selection among said frame delineation methods.

14. The assembly according to claim 10, wherein said third circuit is further configured to provided a plurality of framing methods for a plurality of network protocols.

15. The assembly according to claim 14, further comprising an interface configured to permit a selection among said framing methods.

16. The assembly according to claim 10, wherein said third circuit is further configured to delineate a second receive frame from said second network to produce a second incoming packet.

17. The assembly according to claim 16, wherein said first circuit is further configured to frame a second outgoing packet derived from said second incoming packet to present a second transmit frame to said first network.

18. The assembly according to claim 10, wherein said first circuit comprises a plurality of framing circuits configured to operate on a plurality of network protocols, wherein each one of said framing circuits operates on a corresponding one of said network protocols.

19. The assembly according to claim 10, wherein said third circuit comprises a plurality of de-framing circuits configured to operate on a plurality of network protocols, wherein each one of said de-framing circuits operates on a corresponding one of said network protocols.

20. The assembly according to claim 10, further comprising a fourth circuit connected to said second circuit and configured to process a select one of said first parameters in said incoming packet in accordance with said corresponding pointer value.

IX. EVIDENCE APPENDIX

The following evidence was presented in the Amendment After Final mailed October 23, 2006. Webster's New Collegiate Dictionary, copyright 1979, defines "each one" as a pronoun of "each". The word "each" is defined as "being one of two or more distinct individuals having a similar relation and often constituting an aggregate." The word "only" is defined as "a single fact or instance and nothing more or different."

government in which power is

\dib-ü-'kēm\ *also* **dybbuks**
believed in Jewish folklore to
his actions until exorcised by a

tag; akin to L *fumus* smoke —
ng 2 : a soluble or insoluble

art a new and often permanent
a dye 2 : to impart (a color)
vi : to take up or impart color
t-ē\ *n* — **dye·able** \'dī-ə-bəl\

\ *adj* : THOROUGHGOING, UN-

rüm\ *n, pl* **dyer's–brooms**

ogwood or fustic) from which
ng

mique, fr. Gk *dynamikos* pow-
hai to be able] 1 a : of or
b : of or relating to dynamics
ous usu. productive activity or
ed by energy : FORCEFUL ⟨a ~
l\ *adj* — **dy·nam·i·cal·ly** \-i-

: : DYNAMICS 2
g *or pl in constr* 1 : a branch
and their relation primarily to
the equilibrium of bodies 2
of an object or phenomenon
3 : variation and contrast in

a : a theory that explains the
interplay b : DYNAMICS 2 2
y — **dy·na·mist** \-məst\ *n* —

blasting explosive that is made
us material and that sometimes
ulose nitrate; *also* : a blasting
cerin 2 : one that has explo-
anley Gardner⟩ — **dy·na·mit·ic**

to blow up with dynamite 2
struction of — **dy·na·mit·er** *n*
[short for *dynamoelectric ma-*
eful energetic individual
r\ *n* [F *dynamomètre*, fr. Gk
1 : an instrument for measur-
ratus for measuring mechanical
o·met·ric \-mō-'me-trik\ *adj* —

namo + *motor*] : a motor gen-
and generator
fr. *dynamikos* dynamic (fr. Gk,
at POLICE] : a city planned for
artery
tes, fr. Gk *dynastēs*, fr. *dynasthai*

sp Brit 'din-ə-stē\ *n, pl* **-ties** 1
line of descent 2 : a powerful
position for a considerable time
y·nas·ti·cal·ly \-ti-k(ə-)lē\ *adv*
amis power] : a vacuum tube in
ectrons from the plate results in
e plate voltage increases
the unit of force in the cgs sys-
give a free mass of one gram an
econd per second
] : an electrode in an electron
ndary emission of electrons
fr. MF & L; MF *dis-*, fr. L *dys-*,
t *dus-* bad, difficult] 1 : abnor-
dysphagia⟩ — compare EU- 3
⟨*dys*logistic⟩ — compare EU-
L, fr. ML, bad mixture of hu-
crasis mixture — more at CRASIS]
ly
of or relating to dysentery
-ter·ies [ME *dissenterie*, fr. L
n intestine — more at INTER-] 1
diarrhea with passage of mucus
tion 2 : DIARRHEA
n : impaired or abnormal func-
l, -shən-'l\ *adj*
NL] : defective development esp.
ndrome or Turner's syndrome)
: detrimental to the hereditary
ly defective or deficient
onstr : the study of racial degen-

dys- + Gk *lexis* word, speech]
d — **dys·lex·ic** \-sik\ *adj*
dys- + *-logistic* (as in *eulogistic*)]
-ti·cal·ly \-ti-k(ə-)lē\ *adv*
-ə\ *n* [NL] : painful menstrua-
\ *or* **dys·men·or·rhe·ic** \-'rē-ik\

dys·pep·sia \dis-'pep-shə, -sē-ə\ *n* [L, fr. Gk, fr. *dys-* + *pepsis* digestion, fr. *peptein*, *pessein* to cook, digest — more at COOK] : INDIGESTION

[1]**dys·pep·tic** \-'pep-tik\ *adj* 1 : relating to or having dyspepsia 2 : showing a sour disposition — **dys·pep·ti·cal·ly** \-ti-k(ə-)lē\ *adv*

[2]**dyspeptic** *n* : a person having dyspepsia

dys·pha·gia \dis-'fā-j(ē-)ə\ *n* [NL] : difficulty in swallowing — **dys·phag·ic** \-'faj-ik\ *adj*

dys·pha·sia \dis-'fā-zh(ē-)ə\ *n* [NL] : loss of or deficiency in the power to use or understand language as a result of injury to or disease of the brain — **dys·pha·sic** \-'fā-zik\ *n or adj*

dys·pho·nia \dis-'fō-nē-ə\ *n* [NL] : defective use of the voice — **dys·phon·ic** \-'fän-ik\ *adj*

dys·pho·ria \dis-'fōr-ē-ə, -'fòr-\ *n* [NL, fr. Gk, fr. *dysphoros* hard to bear, fr. *dys-* + *pherein* to bear — more at BEAR] : a state of feeling unwell or unhappy — **dys·phor·ic** \-'fòr-ik, -'fär-\ *adj*

dys·pla·sia \dis-'plā-zh(ē-)ə\ *n* [NL] : abnormal growth or development (as of organs or cells); *broadly* : abnormal anatomic structure due to such growth — **dys·plas·tic** \-'plas-tik\ *adj*

dys·pnea \'dis(p)-nē-ə\ *n* [L *dyspnoea*, fr. Gk *dyspnoia*, fr. *dyspnoos* short of breath, fr. *dys-* + *pnein*, to breathe — more at SNEEZE] : difficult or labored respiration — **dys·pne·ic** \-nē-ik\ *adj*

dys·pro·si·um \dis-'prō-zē-əm, -zh(ē-)əm\ *n* [NL, fr. Gk *dysprositos* hard to get at, fr. *dys-* + *prositos* approachable, fr. *prosienai* to approach, fr. *pros-* + *ienai* to go — more at ISSUE] : an element of the rare-earth group that forms highly magnetic compounds — see ELEMENT table

dys·to·pia \(')dis-'tō-pē-ə\ *n* [NL, fr. *dys-* + *-topia* (as in *utopia*)] : an imaginary place which is depressingly wretched and whose people lead a fearful existence — **dys·to·pi·an** \-pē-ən\ *adj*

dys·tro·phic \dis-'trō-fik\ *adj* 1 : relating to or caused by faulty nutrition 2 *of a lake* : brownish with much dissolved humic matter, a sparse bottom fauna, and a high oxygen consumption

dys·tro·phy \'dis-trə-fē\ *n, pl* **-phies** [NL *dystrophia*, fr. *dys-* + *-trophia* -trophy] : imperfect nutrition; *specif* : any of several neuromuscular disorders — compare MUSCULAR DYSTROPHY

dys·uria \dish-'(y)ùr-ē-ə, dis-'yùr-\ *n* [NL, fr. Gk *dysouria*, fr. *dys-* + *-ouria* -uria] : difficult or painful discharge of urine

dz *abbr* dozen

E

[1]**e** \'ē\ *n, pl* **e's** *or* **es** \'ēz\ *often cap, often attrib* 1 a : the 5th letter of the English alphabet b : a graphic representation of this letter c : a speech counterpart of orthographic *e* 2 : the 3d tone of a C-major scale 3 : a graphic device for reproducing the letter e 4 : one designated *e* esp. as the 5th in order or class; *specif* : the base of the system of natural logarithms having the approximate numerical value 2.71828 5 a : a grade rating a student's work as poor and usu. constituting a conditional pass b : a grade rating a student's work as failing c : one graded or rated with an E 6 : something shaped like the letter E

[2]**e** *abbr, often cap* 1 earth 2 east; easterly; eastern 3 edge 4 eldest 5 ell 6 empty 7 end 8 energy 9 erg 10 error 11 excellent

[3]**e** *symbol* 1 charge of an electron 2 eccentricity of a conic section

E *symbol* 1 einsteinium 2 energy

e- \(')ē, i\ *prefix* [ME, fr. OF & L; OF, out, forth, away, fr. L, fr. *ex-*] 1 a : not ⟨*e*carinate⟩ b : missing : absent ⟨*e*dental⟩ 2 : out : on the outside ⟨*e*scribe⟩ 3 : thoroughly ⟨*e*vaporize⟩ 4 : forth ⟨*e*radiate⟩ 5 : away ⟨*e*luvium⟩

ea *abbr* each

EA *abbr* enemy aircraft

[1]**each** \'ēch\ *adj* [ME *ech*, fr. OE *ǣlc*; akin to OHG *iogilīh* each; both fr. a prehistoric WGmc compound whose first and second constituents respectively are represented by OE *ā* always and by OE *gelīc* alike] : being one of two or more distinct individuals having a similar relation and often constituting an aggregate

[2]**each** *pron* : each one

[3]**each** *adv* : to or for each : APIECE

each other *pron* : each of two or more in reciprocal action or relation ⟨looked at *each other* in surprise⟩

ea·ger \'ē-gər\ *adj* [ME *egre*, fr. OF *aigre*, fr. L *acer* — more at EDGE] 1 a *archaic* : SHARP b *obs* : SOUR 2 : marked by keen, enthusiastic, or impatient desire or interest — **ea·ger·ly** *adv* — **ea·ger·ness** *n*

syn EAGER, AVID, KEEN, ANXIOUS, ATHIRST *shared meaning element* : moved by a strong and urgent desire or interest *ant* listless

eager beaver *n* : one who is extremely zealous in performing his assigned duties and in volunteering for more

ea·gle \'ē-gəl\ *n* [ME *egle*, fr. OF *aigle*, fr. L *aquila*] 1 : any of various large diurnal birds of prey of the accipiter family noted for their strength, size, gracefulness, keenness of vision, and powers of flight 2 : any of various esp. emblematic or symbolic figures or representations of an eagle: as a : the standard of the ancient Romans b : the seal or standard of a nation (as the U.S.) having an eagle as emblem c : one of a pair of silver insignia of rank worn by a military colonel or a navy captain 3 : a ten-dollar gold coin of the U.S. bearing an eagle on the reverse 4 : a golf score of two strokes less than par on a hole — compare BIRDIE 5 *cap* [Fraternal Order of *Eagles*] : a member of a major fraternal order

eagle eye *n* 1 : the ability to see or observe with exceptional keenness 2 : one that sees or observes keenly

eagle ray *n* : any of several widely distributed large active stingrays (family Myliobatidae) with broad pectoral fins like wings

ea·glet \'ē-glət\ *n* : a young eagle

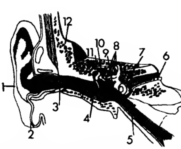
ea·gre \'ē-gər\ *n* [origin unknown] : a tidal bore

eal·dor·man \'al-dər-mən\ *n* [OE — more at ALDERMAN] : the chief officer in a district (as a shire) in Anglo-Saxon England

-ean — see -AN

E and OE *abbr* errors and omissions excepted

[1]**ear** \'i(ə)r\ *n* [ME *ere*, fr. OE *ēare*; akin to OHG *ōra* ear, L *auris*, Gk *ous*] 1 a : the characteristic vertebrate organ of hearing and equilibrium consisting in the typical mammal of a sound-collecting outer ear separated by a membranous drum from a sound-transmitting middle ear that in turn is separated from a sensory inner ear by membranous fenestrae b : any of various organs capable of detecting vibratory motion 2 : the external ear of man and most mammals 3 a : the sense or act of hearing b : acuity of hearing c : sensitivity to musical tone and pitch 4 : something resembling a mammalian ear in shape or position: as a : a projecting part (as a lug or handle) b : either of a pair of tufts of lengthened feathers on the head of some birds 5 a : sympathetic attention b : NOTICE, AWARENESS 6 : a space in the upper corner of a periodical (as a newspaper) usu. containing advertising for the periodical itself or a weather forecast — **by ear** : without reference to or memorization of written music : EXTEMPORANEOUSLY — **in one ear and out the other** : through one's mind without making an impression ⟨everything you say to him goes *in one ear and out the other*⟩ — **on one's ear** : in or into a state of irritation, shock, or discord ⟨his insults really put me *on my ear*⟩ ⟨he set the racing world *on its ear* by breaking 50 world records⟩ — **up to one's ears** : deeply involved : heavily implicated ⟨*up to his ears* in the conspiracy⟩



ear 1a: *1* pinna, *2* lobe, *3* auditory meatus, *4* tympanic membrane, *5* eustachian tube, *6* auditory nerve, *7* cochlea, *8* semicircular canals, *9* stapes, *10* incus, *11* malleus, *12* bones of skull

[2]**ear** *n* [ME *er*, fr. OE *ēar*; akin to OHG *ahir* ear, OE *ecg* edge — more at EDGE] : the fruiting spike of a cereal (as Indian corn) including both the seeds and protective structures

[3]**ear** *vi* : to form ears in the course of growing — often used with *up* ⟨the rye should be ~ing up⟩

ear·ache \'i(ə)r-ˌāk\ *n* : an ache or pain in the ear

ear·drop \-ˌdräp\ *n* : EARRING; *esp* : one with a pendant

ear·drum \-ˌdrəm\ *n* : TYMPANIC MEMBRANE

eared \'i(ə)rd\ *adj* : having ears esp. of a specified kind or number ⟨a big-*eared* man⟩ ⟨golden-*eared* corn⟩

eared seal *n* : any of a family (Otariidae) of seals including the sea lions and fur seals and having independent mobile hind limbs and small well-developed external ears

earflap *n* : a warm covering for the ears; *esp* : an extension on the lower edge of a cap that may be folded up or down

ə abut	ᵊ kitten	ər further	a back	ā bake	ä cot, cart
aù out	ch chin	e less	ē easy	g gift	i trip	ī life
j joke	ŋ sing	ō flow	ò flaw	òi coin	th thin	th this
ü loot	ù foot	y yet	yü few	yù furious	zh vision

'ho is omnipotent 2 *cap* : GOD 1
prez-ˈn(t)s\ *n* : the quality or state of
ITY
present in all places at all times
\ *n* : a system of radio navigation in
'e to a special radio transmitter on the
l flown by an airplane pilot — called also

n(t)s\ *n* [ML *omniscientia*, fr. L *omni-* +
ty or state of being omniscient
[NL *omniscient-*, *omnisciens*, back-
ientia] 1 : having infinite awareness,
2 : possessed of universal or complete
t-ly *adv*
m-nē-əm-ˈgath-ə-rəm\ *n, pl* omnium-
gen. pl. of *omnis*) + E *gather* + L *-um*,
eous collection (as of things or persons)
n pl [NL, fr. L, neut. pl. of *omnivorus*]

-ˌvō(ə)r\ *n* [NL *omnivora*] : one that is

-)rəs\ *adj* [L *omnivorus*, fr. *omni-* +
ng on both animal and vegetable sub-
in everything as if devouring or consum-
'v — **om·niv·o·rous·ness** *n*
an, *on*, prep. & adv., fr. OE; akin to
on] 1 a (1) — used as a function
over and in contact with ⟨the book is ~
function word to indicate a position in
th ⟨a fly ~ the ceiling⟩ (3) — used as a
means of conveyance ⟨left ~ the early
ction word to indicate a part (as of the
in contact with something underneath
— used as a function word to indicate
or area of ⟨~ the right⟩ b (1) — used
ate movement to a position over and in
e horse⟩ (2) — used as a function word
position in contact with ⟨put the notice
— used as a function word to indicate
ied action of a preceding noun, verb, or
r toward the object ⟨crept up ~ him⟩ ⟨a
ports⟩ b : to the disadvantage of ⟨have
— used as a function word to indicate
an action, opinion, or computation)
) ⟨ten cents ~ the dollar⟩ 4 *archaic*
tion word to indicate connection, asso-
with regard to ⟨~ a committee⟩ ⟨~
on word to indicate a state or process of
— used as a function word to indicate
s of a specified day, at a set time, or
ces ⟨came ~ Monday⟩ ⟨every hour ~
7 — used as a function word to indi-
~ a knife⟩ ⟨talking ~ the telephone⟩ 8
to indicate reduplication or succession

n or into a position of contact with an
s ~⟩ b : in or into a position of being
urface ⟨has new shoes ~⟩ 2 a : for-
ion : ONWARD ⟨went ~ home⟩ b : in
⟨and so ~⟩ 3 : into operation or a
n ⟨turn the light ~⟩
ed in an activity or function (as a dra-
ing in operation ⟨the radio is ~⟩ (2)
eration ⟨the switch is ~⟩ b : taking
INTENDED, PLANNED ⟨has nothing ~ for

lter. of *-one*] : chemical compound not
und ⟨parathion⟩
in *ion*)] 1 : elementary particle ⟨nu-
tum ⟨photon⟩ ⟨magneton⟩ b : basic
n⟩ ⟨operon⟩
(in *argon*)] : noble gas ⟨radon⟩
isting briefly and then disappearing in
s way ⟨*on-again, off-again* fads⟩
wild ass, fr. L, fr. Gk *onagros*, fr. *onos*
ACRE] 1 : a small pale-colored kiang
[LL, fr. L] : a heavy catapult used in

prob. fr. NL *onanismus*, fr. *Onan*, son
itus deliberately interrupted to prevent
BATION 3 : SELF-GRATIFICATION —
dj
s, fr. gen. of *on* one] 1 : one time and
: under any circumstances : EVER 3
e past : FORMERLY 4 : by one degree

ORMER
e time at least — **at once** 1 : at the
2 : IMMEDIATELY 3 : ¹BOTH
hen : as soon as
: a swift examination or survey; *esp*
aising glance

r-ˈki-ə-səs\ *n, pl* **-a·ses** \-ˌsēz\ [NL, fr.
] : infestation with or disease caused
ocerca); *esp* : a disease of man caused
is native to Africa but now present in
is transmitted by several biting flies
n, pl **-co·ses** \-ˌsēz\ [NL, fr. *On-*

-ˈkid-\ *n* [NL, genus name, fr. Gk
ANGLE] : any of a genus (*Oncidium*)
piphytic or terrestrial orchids

on·co·gen·e·sis \ˌäŋ-kō-ˈjen-ə-səs\ *n* [NL, fr. Gk *onkos* mass] : the induction or formation of tumors

on·co·gen·ic \-ˈjen-ik\ *adj* 1 : relating to tumor formation 2 : tending to cause tumors

on·co·ge·nic·i·ty \-jə-ˈnis-ət-ē\ *n* : the capacity to induce or form tumors

on·col·o·gy \än-ˈkäl-ə-jē, äŋ-\ *n* [Gk *onkos* mass + ISV *-logy*; akin to Gk *enenkein* to carry — more at ENOUGH] : the study of tumors — **on·co·log·i·cal** \ˌäŋ-kə-ˈläj-i-kəl\ *also* **on·co·log·ic** \-ik\ *adj* — **on·col·o·gist** \än-ˈkäl-ə-jəst, äŋ-\ *n*

on·com·ing \ˈȯn-ˌkəm-iŋ, ˈän-\ *adj* 1 a : coming nearer in time or space ⟨the ~ year⟩ ⟨an ~ car⟩ b : FUTURE ⟨looked forward to his ~ visit⟩ 2 : EMERGENT, RISING ⟨the ~ generation⟩

¹**one** \ˈwən, ˌwən\ *adj* [ME *on*, fr. OE *ān*; akin to OHG *ein* one, L *unus* (OL *oinos*), Skt *eka*] 1 : being a single unit or thing ⟨~ day at a time⟩ 2 a : being one in particular ⟨early ~ morning⟩ b : being preeminently what is indicated ⟨~ fine person⟩ 3 a : being the same in kind or quality ⟨both of ~ species⟩ b (1) : constituting a unified entity of two or more components ⟨the combined elements form ~ substance⟩ (2) : UNITED 4 : existing or occurring as something not definitely fixed or placed ⟨will see you again ~ day⟩ 5 : being the only individual of an indicated or implied kind ⟨the ~ person she wanted to marry⟩ — **at one** : at harmony : in a state of agreement

²**one** *pron* 1 : a certain indefinitely indicated person or thing ⟨saw ~ of his friends⟩ 2 a : an individual of a vaguely indicated group : anyone at all ⟨~ never knows⟩ b — sometimes used as a third person substitute for a first person pronoun ⟨I'd like to read more but ~ doesn't have the time⟩

³**one** \ˈwən\ *n* 1 — see NUMBER table 2 : the number denoting unity 3 : the first in a set or series ⟨wears a ~⟩ 4 : a single person or thing ⟨has the ~ but needs the other⟩ 5 : a one-dollar bill

-one \ˌōn\ *n suffix* [ISV, alter. of *-ene*] : ketone or related or analogous compound or class of compounds ⟨lact*one*⟩ ⟨quin*one*⟩

one another *pron* : EACH OTHER

one-armed bandit \ˌwən-ˌärm(d)-\ *n* *also* **one-arm bandit** *n* : SLOT MACHINE 2

one-bagger \ˈwən-ˈbag-ər\ *n* : SINGLE 2

one-dimensional *adj* : lacking depth : SUPERFICIAL ⟨~ stereotype characters⟩ — **one-dimensionality** *n*

one-egg *adj* : MONOZYGOTIC

one·fold \ˈwən-ˌfōld, -ˈfōld\ *adj* : constituting a single undivided whole

one-hand·ed \-ˈhan-dəd\ *adj* 1 : having or using only one hand ⟨could beat him up ~⟩ 2 a : designed for or requiring the use of only one hand b : effected by the use of only one hand

one-horse *adj* 1 : drawn or operated by one horse 2 : of little real importance or consequence ⟨a ~ town⟩

Onei·da \ō-ˈnīd-ə\ *n, pl* **Oneida** *or* **Oneidas** [Iroquois *Onẽyóde'*, lit., standing rock] 1 a : an Amerindian people orig. of New York b : a member of this people 2 : the language of the Oneida people

onei·ric \ō-ˈnī-rik\ *adj* [Gk *oneiros* dream; akin to Arm *anurj* dream] : of or relating to dreams : DREAMY

onei·ro·crit·i·cal \ō-ˌnī-rō-ˈkrit-i-kəl\ *adj* [Gk *oneirokritikos*, fr. *oneiros* + *kritikos* able to discern — more at CRITIC] : of, relating to, or specializing in the interpretation of dreams — **onei·ro·crit·i·cal·ly** \-k(ə-)lē\ *adv*

onei·ro·man·cy \ō-ˈnī-rə-ˌman(t)-sē\ *n* [Gk *oneiros* + E *-mancy*] : divination by means of dreams

one-line octave *n* : the musical octave that begins on middle C — see PITCH illustration

one-man *adj* : of or relating to just one individual: as a : consisting of only one individual ⟨a ~ committee⟩ b (1) : done, presented, or produced by only one individual ⟨a ~ stage play⟩ b (2) : featuring the work of a single artist (as a painter) ⟨a ~ show of oils⟩ a : designed for or limited to one individual

one·ness \ˈwən-nəs\ *n* : the quality or state or fact of being one: as a : SINGLENESS b : INTEGRITY, WHOLENESS c : HARMONY d : SAMENESS, IDENTITY a : UNITY, UNION

one-night stand *n* 1 : a performance (as of a play or concert) given (as by a traveling group of actors or musicians) only once in each of a series of localities 2 a : a locality used for one-night stands b : a stopover for a one-night stand

one-on-one \ˌwən-ȯn-ˈwən, ˌwən-än-\ *adj* : MAN-TO-MAN 2

one-piece *adj* : consisting of or made in a single undivided piece ⟨a ~ bathing suit⟩ — **one-piec·er** \ˈwən-ˈpē-sər\ *n*

on·er·ous \ˈän-ə-rəs, ˈō-nə-\ *adj* [ME, fr. MF *onereus*, fr. L *onerosus*, fr. *oner-*, *onus* burden; akin to Skt *anas* cart] 1 : involving, imposing, or constituting a burden : TROUBLESOME ⟨an ~ task⟩ 2 : having legal obligations that outweigh the advantages ⟨~ contract⟩ — **on·er·ous·ly** *adv* — **on·er·ous·ness** *n*

syn ONEROUS, BURDENSOME, OPPRESSIVE, EXACTING *shared meaning element* : imposing hardship

one·self \(ˌ)wən-ˈself\ *also* **one's self** \(ˌ)wən-, ˌwənz-\ *pron* 1 : a person's self : one's own self — used reflexively as object of a preposition or verb or for emphasis in various constructions 2 : one's normal, healthy, or sane condition or self — **be oneself** : to conduct oneself in a usual or fitting manner

one-shot \ˈwən-ˌshät\ *adj* 1 : that is complete or effective through being done or used or applied only once ⟨there is no easy ~ answer to the problem⟩ 2 : that is not followed by something else of the same kind ⟨an intensive ~ drive for funds was made⟩

one-sid·ed \ˈwən-ˈsīd-əd\ *adj* 1 a (1) : having or occurring on one side only (2) : having one side prominent or more developed b : limited to one side : PARTIAL ⟨a ~ interpretation⟩ 2 : UNILATERAL ⟨a ~ decision⟩ — **one-sid·ed·ly** *adv* — **one-sid·ed·ness** *n*

one-step \ˈwən-ˌstep\ *n* 1 : a ballroom dance in $\frac{2}{4}$ time marked by quick walking steps backward and forward 2 : music used for the one-step — **one-step** *vi*

one-suit·er \ˈwən-ˈsüt-ər\ *n* : a man's traveling bag designed to hold one suit and accessories

one-tailed test \ˌwən-ˌtāl(d)-\ *n* : a statistical test for which the critical region consists of all values of the test statistic greater than a given value or less than a given value but not both — called also *one-sided test*, *one-tail test*; compare TWO-TAILED TEST

¹**one-time** \ˌwən-ˌtīm\ *adj* : FORMER, SOMETIME

²**onetime** *adv* : FORMERLY

one-to-one \ˌwən-tə-ˈwən, -də-\ *adj* : pairing each element of a set uniquely with an element of another set

one-track *adj* : marked by often narrowly restricted attention to or absorption in just one thing ⟨a ~ mind⟩

one-two \ˈwən-ˈtü, -ˌtü\ *n* : a combination of two quick blows in rapid succession in boxing; *esp* : a left jab followed at once by a hard blow with the right hand

one-up \ˌwən-ˈəp, ˈwən-\ *vt* [back-formation fr. *one-upmanship*] : to practice one-upmanship on

one up *adj* : being in a position of advantage — usu. used with *on*

one-up·man·ship \ˌwən-ˈəp-mən-ˌship\ *n* : the art or practice of going a friend or competitor one better or keeping one jump ahead of him

one-way *adj* 1 : that moves in or allows movement in only one direction ⟨~ traffic⟩ 2 : ONE-SIDED, UNILATERAL ⟨a ~ conversation⟩ 3 : that functions in only one of two or more ways

on·go·ing \ˈȯn-ˌgō-iŋ, ˈän-, -ˌgō(-)iŋ\ *adj* 1 : being actually in process 2 : continuously moving forward : GROWING

ONI *abbr* Office of Naval Intelligence

on·ion \ˈən-yən\ *n* [ME, fr. MF *oignon*, fr. L *union-*, *unio*] 1 : a widely cultivated Asiatic herb (*Allium cepa*) of the lily family with pungent edible bulbs; *also* : its bulb 2 : any of various plants of the same genus as the onion

on·ion·skin \-ˌskin\ *n* : a thin strong translucent paper of very light weight

oni·um \ˈō-nē-əm\ *adj* [*-onium*] : being or characterized by a usu. complex cation

-o·ni·um \ˈō-nē-əm\ *n suffix* [NL, fr. *ammonium*] : an ion having a positive charge ⟨ox*onium*⟩ — compare -IUM 1b

on-line *adj* 1 : located at a point served directly by a particular railroad ⟨~ industry⟩ 2 : being controlled directly by or in direct communication with a computer ⟨~ equipment⟩ 3 : of, relating to, or being a cryptographic system whose telecommunication machines automatically encipher, transmit, receive, and decipher messages in a single instantaneous operation — compare OFF-LINE — **on-line** *adv*

on·look·er \ˈȯn-ˌlu̇k-ər, ˈän-\ *n* : one that looks on; *esp* : a passive spectator — **on·look·ing** \-iŋ\ *adj*

¹**on·ly** \ˈōn-lē\ *adj* [ME, fr. OE *ānlic*, fr. *ān* one — more at ONE] 1 : unquestionably the best : PEERLESS 2 : alone in its class or kind : SOLE ⟨an ~ child⟩

²**only** *adv* 1 a : as a single fact or instance and nothing more or different : MERELY ⟨has ~ lost one election —George Orwell⟩ b : SOLELY, EXCLUSIVELY ⟨known ~ to him⟩ 2 : at the very least ⟨it was ~ too true⟩ 3 a : in the final outcome ⟨will ~ make you sick⟩ b : with nevertheless the final result ⟨won the battles, ~ to lose the war⟩ 4 a : as recently as ⟨~ last week⟩ b : in the immediate past ⟨~ just talked to her⟩

³**only** *conj* 1 a : with the restriction that : BUT ⟨you may go, ~ come back early⟩ b : and yet : HOWEVER ⟨they look very nice, ~ we can't use them⟩ 2 : were it not that : EXCEPT

on·o·mas·tic \ˌän-ə-ˈmas-tik\ *adj* [Gk *onomastikos*, fr. *onomazein* to name, fr. *onoma* name — more at NAME] 1 : of, relating to, or consisting of a name or names 2 *of a signature* : written in the handwriting of the author of a letter or document the body of which is in the handwriting of another person

on·o·mas·tics \-tiks\ *n pl but sing or pl in constr* 1 a : the science or study of the origins and forms of words esp. as used in a specialized field b : the science or study of the origin and forms of proper names of persons or places 2 : the system underlying the formation and use of words esp. for proper names or of words used in a specialized field

on·o·ma·tol·o·gy \ˌän-ə-mə-ˈtäl-ə-jē\ *n* [F *onomatologie*, fr. Gk *onomat-*, *onoma* name + F *-logie* -logy] : ONOMASTICS

on·o·mato·poe·ia \ˌän-ə-ˌmat-ə-ˈpē-(y)ə\ *n* [LL, fr. Gk *onomatopoiia*, fr. *onomat-*, *onoma* name + *poiein* to make — more at POET] 1 : the naming of a thing or action by a vocal imitation of the sound associated with it (as *buzz*, *hiss*) 2 : the use of words whose sound suggests the sense — **on·o·mato·poe·ic** \-ˈpē-ik\ *or* **on·o·mato·po·et·ic** \-pō-ˈet-ik\ *adj* — **on·o·mato·poe·i·cal·ly** \-ˈpē-ə-k(ə-)lē\ *or* **on·o·mato·po·et·i·cal·ly** \-pō-ˈet-i-k(ə-)lē\ *adv*

On·on·da·ga \ˌän-ə(n)-ˈdȯ-gə\ *n, pl* **Onondaga** *or* **Onondagas** [Iroquois *Onõtáge*, village of the Onondaga people] 1 a : an Amerindian people of New York and Canada b : a member of this people 2 : the language of the Onondaga people

ONR *abbr* Office of Naval Research

on·rush \ˈȯn-ˌrəsh, ˈän-\ *n* 1 : a rushing forward or onward 2 : ONSET — **on·rush·ing** \-iŋ\ *adj*

on·set \-ˌset\ *n* 1 : ATTACK, ASSAULT ⟨withstand the ~ of the army⟩ 2 : BEGINNING, COMMENCEMENT ⟨the ~ of winter⟩ — **on·set·ting** \-ˌset-iŋ\ *adj*

on·shore \ˈȯn-ˌshō(ə)r, ˈän-, -ˌshȯ(ə)r\ *adj* 1 : coming or moving toward or onto the shore ⟨an ~ wind⟩ 2 a : situated on or near the shore b : DOMESTIC ⟨~ oil production⟩ ⟨~ purchases⟩ — **onshore** \ˈȯn-ˈ, ˈän-ˈ\ *adv*

on·side \-ˈsīd\ *adv or adj* : not off side : in a position legally to play or receive the ball or puck

onside kick *n* : a kickoff in football in which the ball travels just far enough to be legally recoverable by the kicking team

on·slaught \ˈän-ˌslȯt, ˈȯn-\ *n* [modif. of D *aanslag* act of striking; akin to OE *an* on and to OE *slēan* to strike — more at SLAY] : an esp. fierce attack

ə abut	ˈ kitten	ər further	a back	ā bake	ä cot, cart	
au̇ out	ch chin	e less	ē easy	g gift	i trip	ī life
j joke	ŋ sing	ō flow	ȯ flaw	ȯi coin	th thin	t͟h this
ü loot	u̇ foot	y yet	yü few	yu̇ furious	zh vision	

X. RELATED PROCEEDINGS APPENDIX

None.